ADM-XRC-9Z1
User Manual

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	Head Office	US Office
Address:	Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK	10822 West Toller Drive, Suite 250 Littleton, CO 80127
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

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1 Introduction

The ADM-XRC-9Z1 is a high-performance XMC for applications the Zynq Ultrascale+ MPSoC from Xilinx.

The ADM-XRC-9Z1 is available in air-cooled and conduction-cooled configurations. View the Ordering Info tab at ADM-XRC-9Z1 Product Page on www.alpha-data.com.

1.1 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0, 42.3 and 42.10d12
- Support for Zynq Ultrascale+ ZU7EG, ZU7EV and ZU11EG devices in FFVF1517 packages
- Voltage and temperature monitoring,
- Air-cooled and conduction-cooled configurations,
- Micro USB System platform manager with voltage and temperature measurements
- Processing System (PS) Block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 PS bank of 72-bit wide DDR4-2400 SDRAM 8GB with ECC
  - Removable microSD Flash memory
  - 8-bit wide EMMC flash memory, 32GB
  - 8-bit wide Quad SPI Flash memory, 2Gb
  - 2 USB 2.0 ports to rear P4 connector
  - 2 Gigabit Ethernet interfaces to rear P4 connector
  - 1 CAN bus interface to rear P4 connector
  - 1 serial COM port interface to rear P4 connector (configurable as either RS-232 or RS-422/485)
  - 4 single ended PS GPIO pins to the P4 connector
  - 4 GTR lanes to the P5 or P6 connectors
- Programmable Logic (PL) block consisting of:
  - Standard XRM2 IO Interface to FPGA
  - 10 HSSIO links to the P6 connector, 16Gbps capable
  - 8 HSSIO links to the P5 connector
  - 2 banks of 32-bit wide DDR4-2666 SDRAM, 4GB per bank
  - 1 serial COM port interface to rear P4 connector (configurable as either RS-232 or RS-422/485)
  - 38 single ended GPIO pins to the P6 connector
  - 6 differential (or 12 single ended) 1.8V GPIO pins to the P4 connector

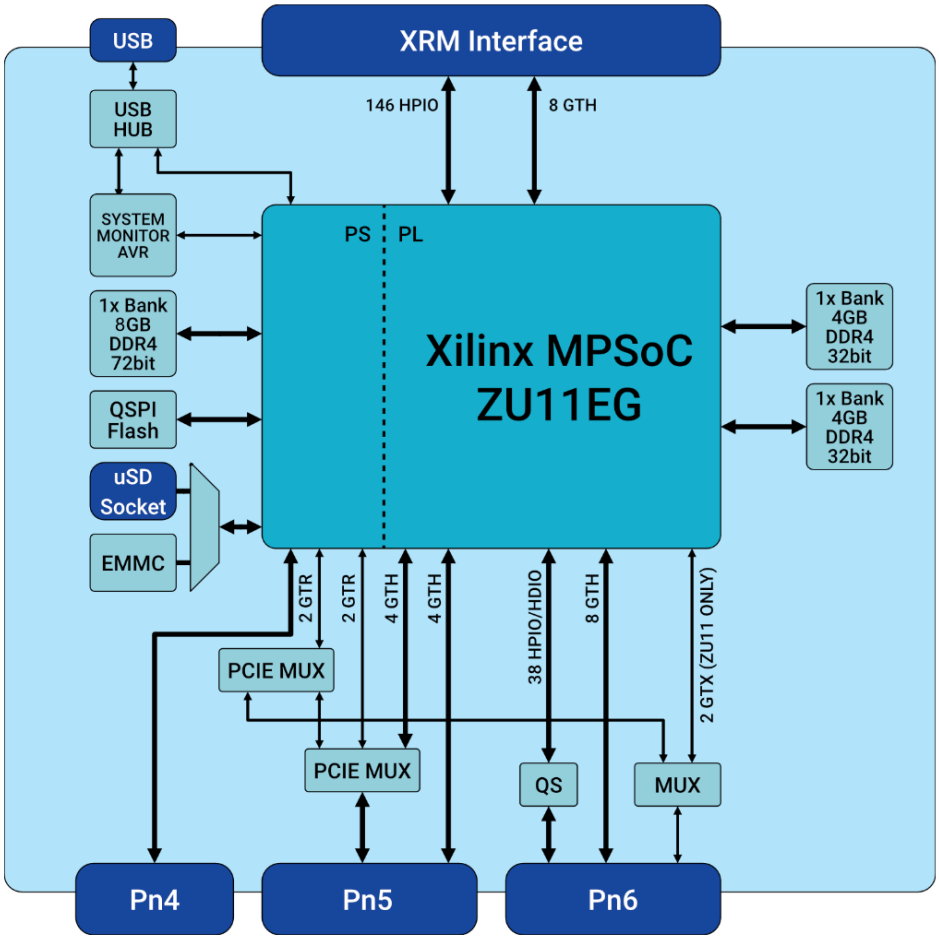


Figure 1 : ADM-XRC-9Z1 Block Diagram

1.2 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.2	*XMC Serial RapidIO Protocol Layer Standard*, Feb 2006, VITA, ISBN 1-885731-41-8
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/VITA 46.9	*PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 1 : References

2 Installation

2.1 Hardware Installation

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.1.2 Motherboard / Carrier Requirements

The ADM-XRC-9Z1 is a single width XMC.3 mezzanine with P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

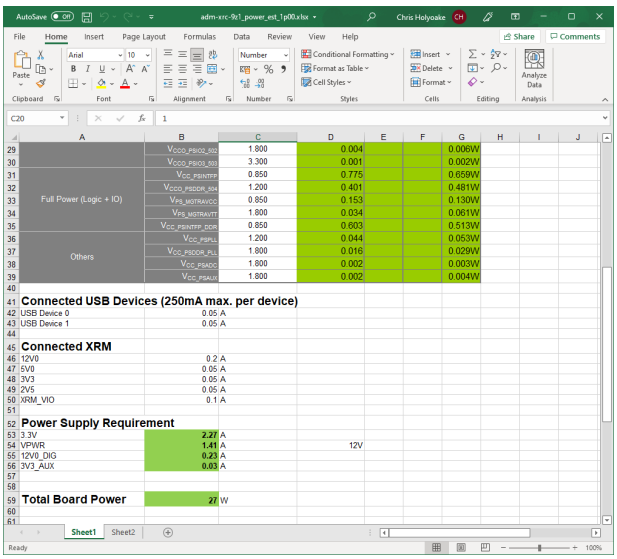
The Secondary XMC connector, P6 has a pinout compatible with various XMC to VPX signal maps as defined by VITA 46.9. Please consult the pinouts in this user-guide as-well as those of the carrier manufacturer prior to installation. Assistance can be provided by Alpha Data.

IMPORTANT
Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The ADM-XRC-9Z1 is compatible with either 5V or 12V on the "VPWR" power rail.

2.1.3 Cooling Requirements

The power dissipation of the board is highly dependent on the FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.



	$V_{CCO\_PSIO1\_503}$	1.800	0.004			0.006W
	$V_{CCO\_PSIO1\_503}$	3.300	0.001			0.002W
	$V_{CC\_PSINTFP}$	0.850	0.775			0.659W
Full Power (Logic + IO)	$V_{CCO\_PSDDR\_504}$	1.200	0.401			0.481W
	$V_{PS\_MGTRAVCC}$	0.850	0.153			0.130W
	$V_{PS\_MGTRAVTT}$	1.800	0.034			0.061W
	$V_{CC\_PSINTFP\_DDR}$	0.850	0.603			0.513W
	V_{CC_PSPLL}	1.200	0.044			0.053W
Others	$V_{CC\_PSDDR\_PLL}$	1.800	0.016			0.029W
	V_{CC_PSADC}	1.800	0.002			0.003W
	V_{CC_PSAUX}	1.800	0.002			0.004W
Connected USB Devices (250mA max. per device)						
USB Device 0		0.05 A				
USB Device 1		0.05 A				
Connected XRM						
12V0		0.2 A				
5V0		0.05 A				
3V3		0.05 A				
2V5		0.05 A				
XRM_VIO		0.1 A				
Power Supply Requirement						
3.3V		**2.27** A				
VPWR		**1.41** A		12V		
12V0_DIG		**0.23** A				
3V3_AUX		**0.03** A				
Total Board Power		**27** W				

Figure 2 : Alpha Data Power Estimator Spreadsheet

The board is supplied with a passive air cooled or conduction cooled heat-sink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the FPGA configuration if an over-temperature condition is detected.

See Section 3.9 for further details.

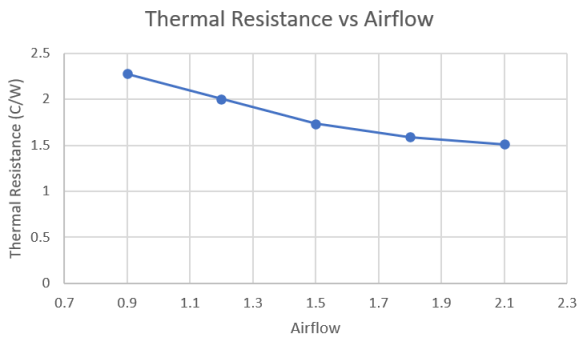


Figure 3 : Air Cooled Heatsink Performance vs Airflow

3 Functional Description

3.1 Overview

3.1.1 Switch Definitions

There are two sets of eight DIP switches (16 switches in total) placed on the rear of the board. Some switch states can be controlled using the FPGA or the AVR system monitor. These signals are shown in the corresponding table. Signals controllable by the system monitor can be controlled using the AVR2Util utility (See Section 3.9.3 for information on using AVR2Util).

The default switch states for SD card boot mode are SW1[8:1]:00000001 and SW2[8:1]:00001100. SW2-6 can either be ON or OFF depending on whether the card is used with a carrier with a JTAG connection to the XMC site.

Note:
Factory Configuration switch (SW2-5) must be in the OFF position for normal operation.

Switch Ref.	Function	FPGA Pin	ON State	Off State
SW1-1	P5 GT Select	B11	See Table 14	
SW1-2	P6 GT Select	B10	See Table 14	
SW1-3	UART1 RS485 Enable	A10	UART1 RS485	UART1 RS232
SW1-4	UART2 RS485 Enable	A12	UART2 RS485	UART2 RS232
SW1-5	MRSTO Disable	-	MRSTO pulled high	MRSTO driven by PL
SW1-6	P4 GPIO Enable	A11	P4 GPIO Enabled	P4 GPIO Disabled
SW1-7	SD/EMMC Select	-	SD Card Boot	EMMC Boot
SW1-8	Unused	-	-	-

Table 2 : SW1 Switch Definitions

Switch Ref.	Function	AVR Control	FPGA Pin	ON State	Off State
SW2-1	BootMode 0	Yes	-	See Table 11	
SW2-2	BootMode 1	Yes	-	See Table 11	
SW2-3	BootMode 2	Yes	-	See Table 11	
SW2-4	BootMode 3	Yes	-	See Table 11	
SW2-5	*Factory Configuration*	No	-	-	Normal Operation
SW2-6	XMC JTAG Enable	Yes	-	XMC JTAG interface is enabled	XMC JTAG interface is disabled

Table 3 : SW2 Switch Definitions (continued on next page)

Switch Ref.	Function	AVR Control	FPGA Pin	ON State	Off State
SW2-7	XMC PCIE reset enable	No	-	XMC PCIE reset connected from PS	XMC PCIE reset disconnected to PS
SW2-8	PS Reset	Yes	-	PS is held in reset	Normal Operation

Table 3 : SW2 Switch Definitions

Pins controlled by the system monitor are non-volatile, allowing the Boot Mode and other configurations to be stored between power cycles[1]. Some signals can also be controlled by the FPGA. If a signal needs to be turned ON, the FPGA pin listed in the table should be pulled LOW. If the signal needs to be turned off, the FPGA pin should be left to float, either with a tristate buffer instantiated in the FPGA, or by not including these signals in the FPGA design at all. The Example Switch Control Circuit diagram shows a typical switch circuit. The 500R pull-down resistor is used to ensure that the FPGA or AVR output pins are never shorted to ground in case the switch is ON while the FPGA/AVR is driving a high output.

[1]: If the boot mode is overridden by the system monitor, then 3V3_AUX must be applied before power up in order to ensure the pins are configured before the Zynq PS boot mode pins are sampled. If 3V3_AUX is powered up at the same time as the main power, an incorrect boot mode may be selected.

SW1-2 is used as an example, but other switches that can be controlled from the FPGA and AVR use a similar circuit.

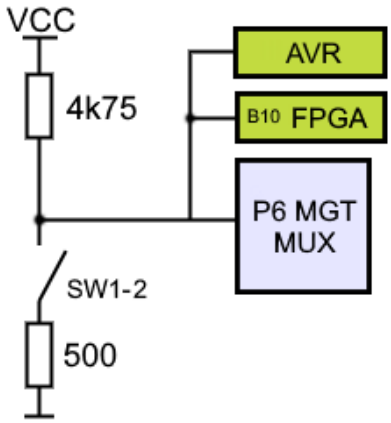


Figure 4 : Example Switch Control Circuit

3.1.2 LED Definitions

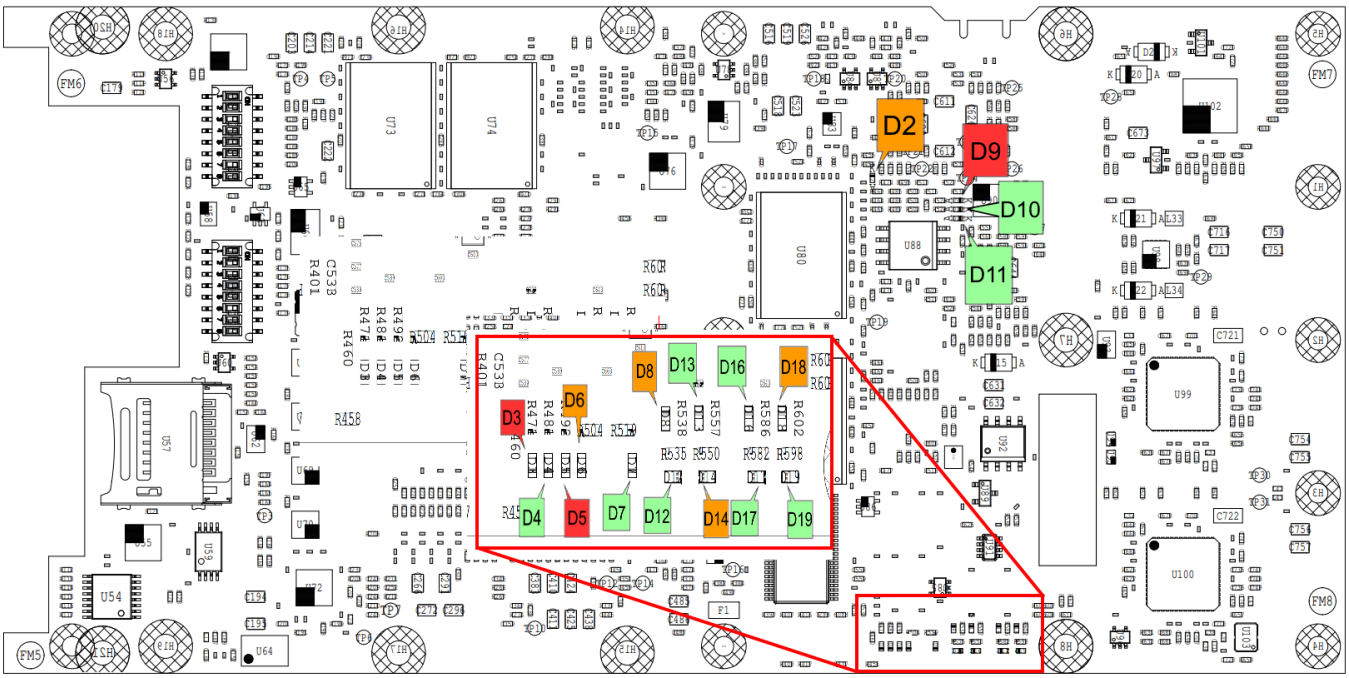


Figure 5 : LED Locations

Comp. Ref.	Function	ON State	Off State
D1(Green)	XRM Power OK	XRM power OK	XRM is unpowered or XRM power fault
D2(Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories
D3(Red)	Power Fault	Power supply fault	Normal operation
D4(Green)	Status 0	See Status LED Definitions	
D5(Red)	Status 1	See Status LED Definitions	
D9(Red)	PS Error	PS error occurred	No PS error
D10(Green)	PS Error Status	PS is in secure lockdown state	PS is operating normally
D11(Green)	Done	FPGA is configured	FPGA is unconfigured
D6(Amber)	Eth0 Status	See Ethernet Status LEDs	
D7(Green)	Eth0 Status	See Ethernet Status LEDs	
D12(Green)	Eth0 Status	See Ethernet Status LEDs	
D14(Amber)	Eth1 Status	See Ethernet Status LEDs	
D17(Green)	Eth1 Status	See Ethernet Status LEDs	
D19(Green)	Eth1 Status	See Ethernet Status LEDs	
D8(Amber)	USB0 Status	USB0 port over current	USB0 port normal
D16(Green)	USB0 Status	USB0 port enabled	USB0 port not enabled
D18(Amber)	USB1 Status	USB1 port over current	USB1 port normal
D13(Green)	USB1 Status	USB1 port enabled	USB1 port not enabled

Table 4 : LED Definitions

3.2 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two Samtec connectors, CN1 and CN2.

3.2.1 XRM Connector, CN1

Connector CN1 is for general purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the ADM-XRC-9Z1 is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in XRM Connector CN1, Field 1 to XRM Connector CN1, Field 3.

3.2.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the ADM-XRC-9Z1 is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in XRM Connector CN2.

3.2.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that can be either 1.8V, 1.5V or 1.2V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	16-17	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	15-16	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	15	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	17	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 5 : XRM GPIO Groups

3.2.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

3.2.5 XRM IO Voltage Override

Each XRM is built with an I2C EEPROM that contains vital product information (VPD) such as part number, serial number, operating voltage, and product specific information. For designing custom XRMs, contact Alpha-Data for details on duplicating this VPD data.

Alternatively, FORCE2V5_L can be driven low to select 1.8V for the front I/O voltage. Note that FORCE2V5_L is a signal name from a historical design, and the operating voltage will not be 2.5V but rather 1.8V if this mode is used.

3.3 XMC Platform Interface

3.3.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

3.3.2 MBIST#

Built-In Self Test. This output signal is connected to FPGA pin AW24. It is not driven by default, and has a 4.75kOhm pull-up resistor.

3.3.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D2.

The MVMRO signal has a 100KΩ pull-up resistor fitted by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the FPGA at pin AV27.

3.3.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. A this signal connected to the PS at pin L30. This signal can also drive the PS power-on-reset pin depending on SW1-7

A buffered version of MRSTI# is also connected to the FPGA at pin AU25.

3.3.5 MRSTO#

XMC Reset Out. This optional output signal is driven from the FPGA pin AV23. This signal is passed through a tristate buffer controlled by SW1-5 to optionally isolate the FPGA from MRSTO. There are pull-ups on both sides of the buffer so that MRSTO is always de-asserted unless the FPGA actively drives it low.

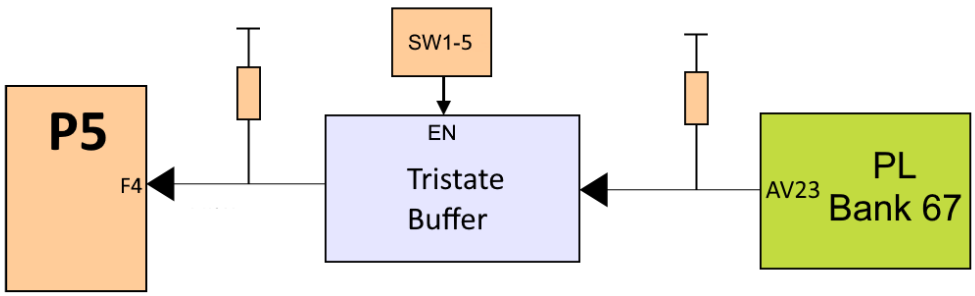


Figure 6 : MRSTO Circuit

3.3.6 MPRESENT#

Module Present. This output signal is connected directly to GND.

3.4 JTAG Interface

3.4.1 On-board JTAG Interface

A JTAG boundary scan chain is connected to header U35. This allows the connection of a Xilinx JTAG cable for FPGA debug using the Xilinx tools. The ADM-XRC-9Z1 comes with an adaptor board to attach to this connector, providing access to a standard 14-pin JTAG header that is compatible with the Xilinx Platform II JTAG box. The adaptor board connects through holes in the rear of the PCB so that the JTAG chain can be accessed while the board is attached to a carrier.

The JTAG Header location is shown in JTAG Header U35:

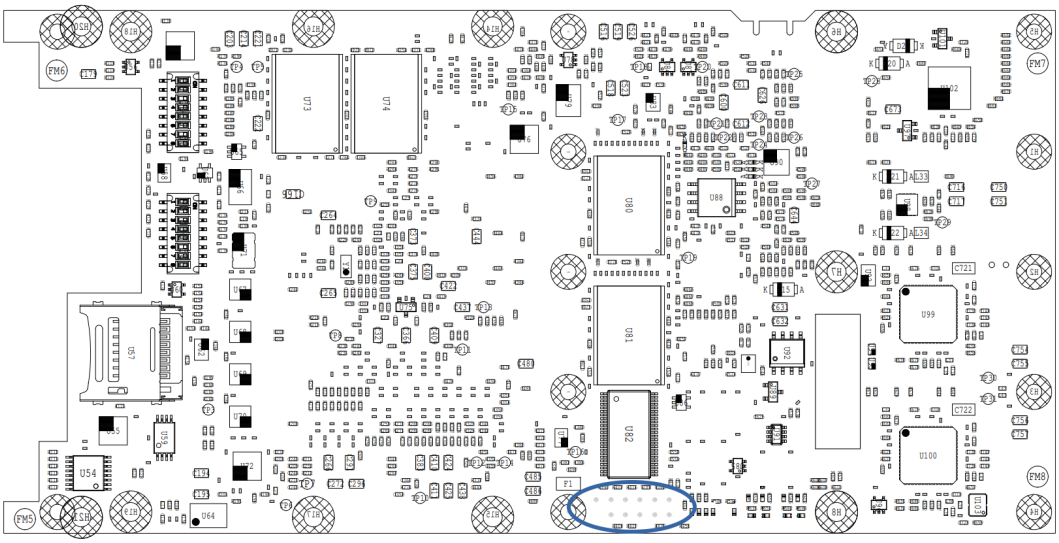


Figure 7 : JTAG Header U35

The scan chain is shown in JTAG Boundary Scan Chain:

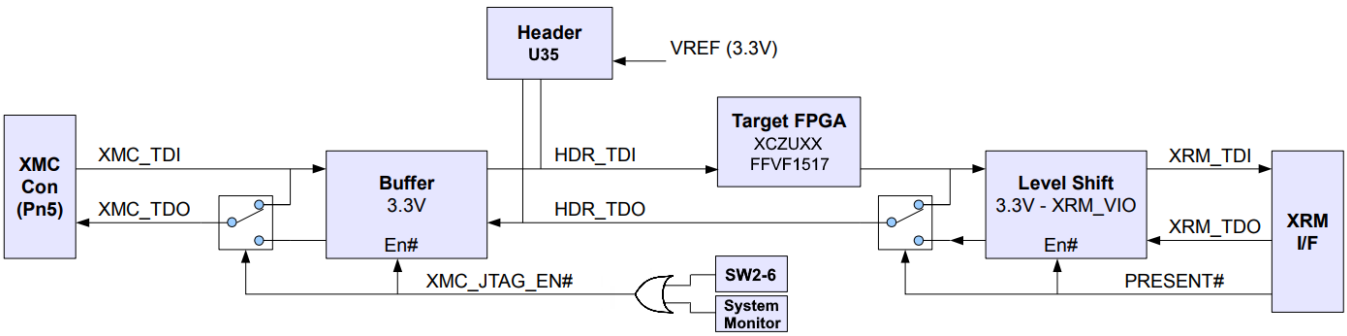


Figure 8 : JTAG Boundary Scan Chain

SW2-6 controls whether the JTAG interface connects to U35, or to the P5 XMC connector. This can also be controlled using the on-board AVR system-monitor, either using the micro USB interface or from the Zynq PS using the on-board serial interface between the PS and the AVR. If the boundary scan chain is connected to the interface at the XMC connector (SW2-6 is ON), header U35 is disconnected.

3.4.2 XMC JTAG Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The clock line on this JTAG interface (XMC_TCK) has a parallel termination (49.9Ω + 22pF to ground) located underneath the 3.3V buffer (U1).

The interface can be connected to the on-board interface (through level-translators) by switching SW1-5 ON. See Switch Definitions

3.4.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The VCC supply provided on J2 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 375mA.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM interface use the adjustable voltage XRM_VIO.

3.5 Clocks

The ADM-XRC-9Z1 provides a wide variety of clocking options, using some fixed oscillators and a user-programmable clock generator. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

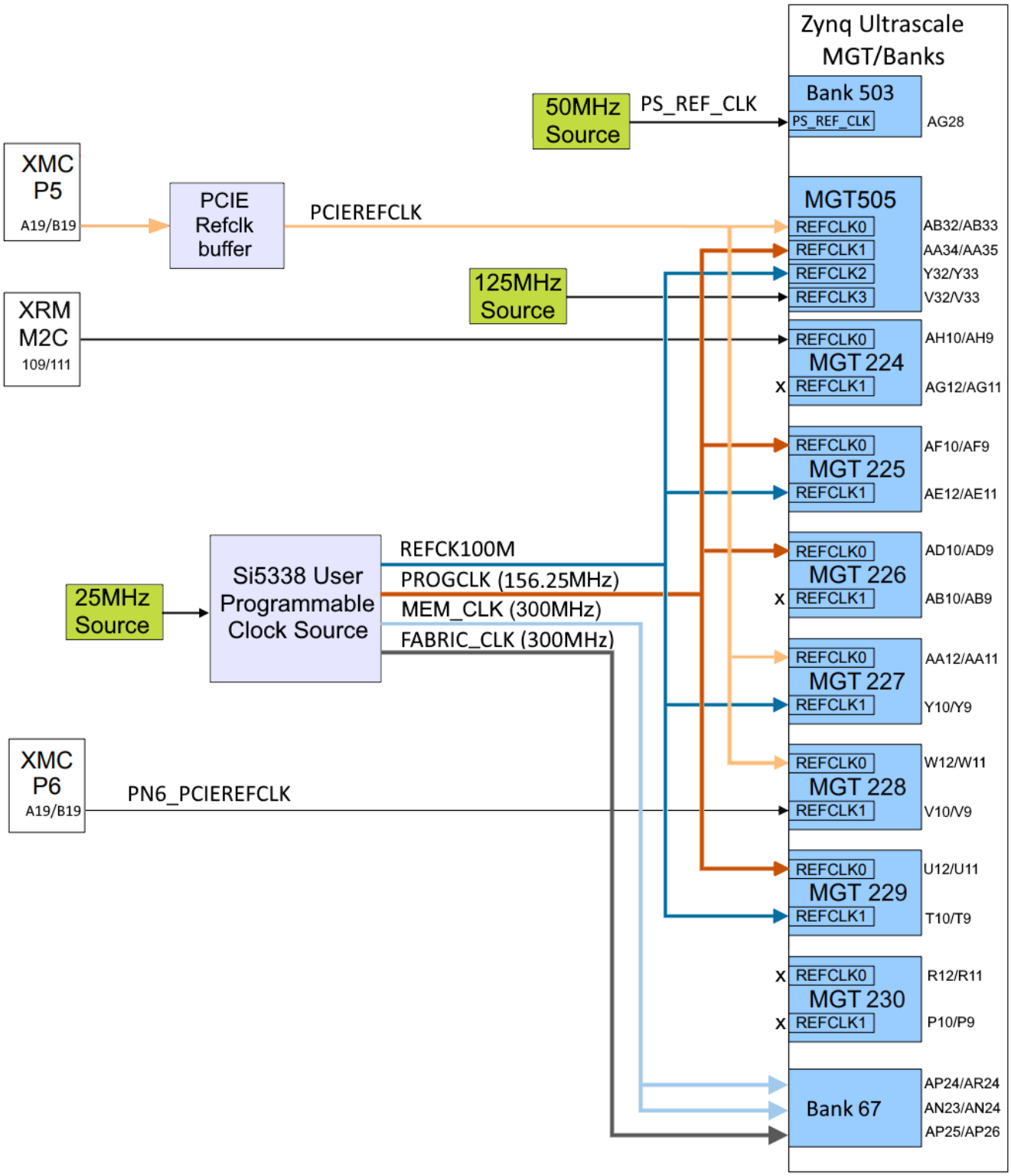


Figure 9 : Board Clock Diagram

3.5.1 300MHz Reference Clocks (MEM_CLK and FABRIC_CLK)

The fixed 300MHz reference clocks MEM_CLK and FABRIC_CLK are differential LVDS signals.

MEM_CLK0 is used as the input clock for both DDR4 SDRAM interfaces.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
MEM_CLK0	300 MHz	IO_L12_T1U_N10_-GC_67	LVDS	AP24	AR24
MEM_CLK1	300 MHz	IO_L13_T2L_N0_G-C_QBC_67	LVDS	AN23	AN24
FABRIC_CLK	300 MHz	IO_L11_T1U_N8_GC_67	LVDS	AP25	AP26

Table 6 : 300MHz Connections

3.5.2 PCIe Reference Clocks (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector P5 at pins A19 and B19. This clock is buffered into two PCIe Express reference clocks that are forwarded to the PS GTR and PL GTY transceivers.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK0	100 MHz	PS_MGTREFCLK0_505	LVDS	AB32	AB33
PCIEREFCLK1	100 MHz	MGTREFCLK1_227	LVDS	AA12	AA11
PCIEREFCLK2	100 MHz	MGTREFCLK1_228	LVDS	W12	W11

Table 7 : PCIEREFCLK Connections

3.5.3 PN6 Reference Clock (PN6_PCIEREFCLK)

The reference clock "PN6_PCIEREFCLK" is a differential clock provided by a carrier card through the Secondary XMC connector P6 at pins A19 and B19. This board connects this pair to an MGT clock input.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PN6_PCIEREFCLK	Carrier Defined	MGTREFCLK1_228	LVDS	V10	V9

Table 8 : PN6_PCIEREFCLK Connections

3.5.4 Programmable Clocks (PROGCLK 0-3)

There is one programmable clock source that is forwarded throughout the FPGA. This clock is programmable through the USB system monitor. PROGCLK[2:0] is generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments). PROGCLK[3:0] are all buffered copies of the same clock signal.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK0	5 - 312.5 MHz	PS_MGTREFCLK1_505	LVDS	AA34	AA35
PROGCLK1	5 - 312.5 MHz	MGTREFCLK0_225	LVDS	AF10	AF9
PROGCLK2	5 - 312.5 MHz	MGTREFCLK0_226	LVDS	AD10	AD9
PROGCLK3	5 - 312.5 MHz	MGTREFCLK0_229	LVDS	U12	U11

Table 9 : PROGCLK Connections

3.5.5 Fixed Oscillators

There are five fixed oscillators on the board for the digital system. The USB and Ethernet reference clocks are used internally by the PHYs.

Signal	Frequency	FPGA pin
GTR Refclk	125MHz	V32/V33 (PS GTR Refclk 3)
PS Ref Clock	50MHz	AG28
Si5338 Ref Clock	25MHz	-
USB Ref Clock	24MHz	-
Ethernet Ref Clock	25MHz	-

Table 10 : Reference clocks Connections

3.6 Zynq PS Block

3.6.1 Boot Modes

BootMode0 (SW2-1)	BootMode1 (SW2-2)	BootMode2 (SW2-3)	BootMode3 (SW2-4)	Boot Mode
ON	ON	ON	ON	JTAG
ON	OFF	ON	ON	Quad SPI
OFF	OFF	ON	ON	SD Flash
-	-	-	-	Reserved

Table 11 : Boot Mode Selection

3.6.2 Quad SPI Flash Memory

1Gb Flash Memory (2x Micron MT25QU512AB) is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream.

The flash memory can only be accessed by the PS.

Utilities for erasing, programming and verification of the flash memory are available in Linux.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED as shown in LED Locations.

3.6.3 MicroSD Flash Memory

A MicroSD card is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream. The SD card is attached to a multiplexer with the EMMC to select either the SD Card or EMMC as the boot device, controlled by SW1-7.

The SD Card can only be accessed by the PS.

3.6.4 EMMC Flash Memory

An EMMC device is provided for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream. The EMMC is attached to a multiplexer with the SD card to select either the SD Card or EMMC as the boot device, controlled by SW1-7.

The EMMC memory can only be accessed by the PS.

3.6.5 PS DDR4 Memory

The ADM-XRC-9Z1 is fitted with one bank of PS DDR4 SDRAM. The bank is made up of a five 16-bit wide memory devices in parallel to provide a 72-bit data-path capable of running up to 1200MHz (DDR4-2400). 2GByte devices (Micron MT40A1G16RC-062) are fitted as standard to provide 8GByte of memory with ECC.

Full details of the interface, signalling standards and an example design are provided in the ADM-XRC-9Z1 example design.

3.6.6 PS MGT Links

There are a total of 4 MGT links connected to the PS Multi-Gigabit Transceivers. These MGT links are routed through multiple layers of muxing to allow flexible PCIE options. See MGT Links for further details.

3.6.7 Ethernet Interfaces

The **9Z1** has two 1000BASE-T Ethernet interfaces at rear connector P4.

Both interfaces have a Marvell 88E1512 PHY, connected to the Zynq via RGMII.

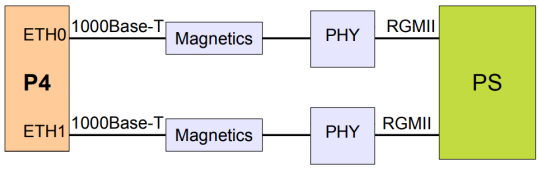


Figure 10 : Ethernet Interfaces

Each interface has three status LEDs. The functions of these are shown in Table 12 below.

Eth0 LED	Eth1 LED	Colour	Function
D12	D19	Green	On = Link up
D7	D17	Green	Unused
D6	D14	Amber	On = Link up

Table 12 : Ethernet Status LEDs

3.6.8 Serial COM Ports

There is one PS COM port connected to PMC connector P4, as shown in Figure Serial COM Ports. The default speed of this COM port is 115.2k.

The COM ports use RS-232 by default but may be configured for RS-485, controlled by SW1-3 and SW1-4. When in RS-485 mode, the pinout of any external COM ports may not be standard

The System monitor UART connects to both the PS and the PL, so the unused interface must be tri-stated to avoid IO pin conflicts.

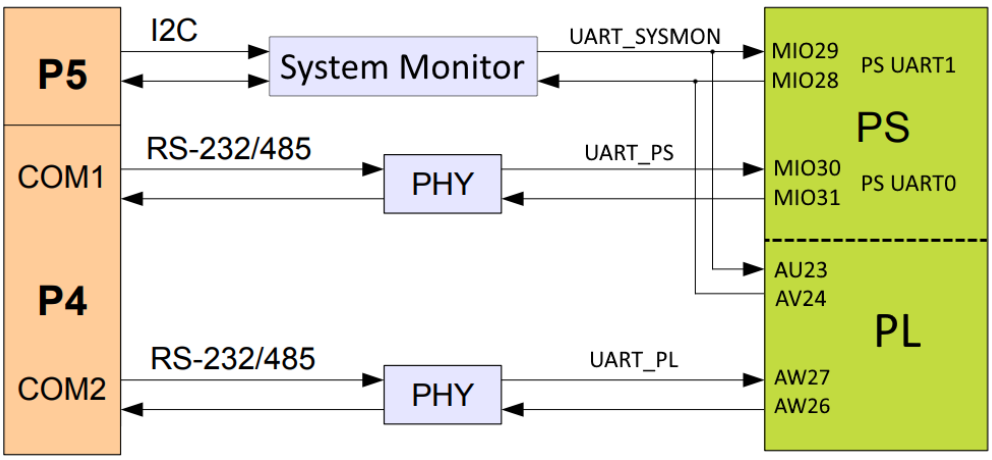


Figure 11 : Serial COM Ports

3.6.9 USB Interfaces

The ADM-XRC-9Z1 has two external USB interfaces connected to rear connector P4.

The Zynq PS is configured as the USB host to the external interfaces.

The on-board system monitor is accessible from the micro-USB connector

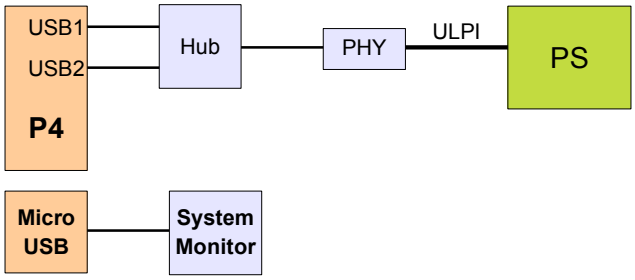


Figure 12 : USB Interfaces

3.6.10 PS GPIO

There are 4 single ended GPIO pins from the PS to the P4 connector, which are compatible with 3.3V signalling such as TTL and CMOS. These GPIO pins are passed through a Texas Instruments TXS0108E level translator, capable of open-drain and push-pull level translation. The level translator is auto direction sensing. The level translator has a propagation delay of 5.7ns max and a channel-to-channel skew (within a package) of 1ns. It is suitable for rates up to ~50Mb/s.

The PS GPIO is shown in GPIO Block Diagram.

3.7 PL Interfaces

3.7.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with their own power supply pins. The bank numbers, their voltage and function are shown in FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the xdc constraints files of ADM-XRC-9Z1 example designs.

IO Banks	Voltage	Purpose
503	3.3V	Configuration, JTAG, Boot Mode Select
88, 89	3.3V	SE GPIO, Board Control
67	1.8V	Diff. GPIO, Board Control
64, 65, 66	Variable	XRM IO
68, 69	1.2V	PL DDR Bank 0
70, 71	1.2V	PL DDR Bank 1

Table 13 : FPGA IO Banks

3.7.2 Memory Interfaces

The ADM-XRC-9Z1 has two independent banks of DDR4 SDRAM. Each bank consists of two 16-bit wide memory device capable of running at up to 1333MHz (DDR-2666). 16Gbit devices (Micron MT40A1G16RC-062E) are fitted as standard.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). PL DRAM Banks shows the component references and FPGA banks used. Full details of the interface, signalling standards and an FPGA design are provided in the ADM-XRC-9Z1 example design.

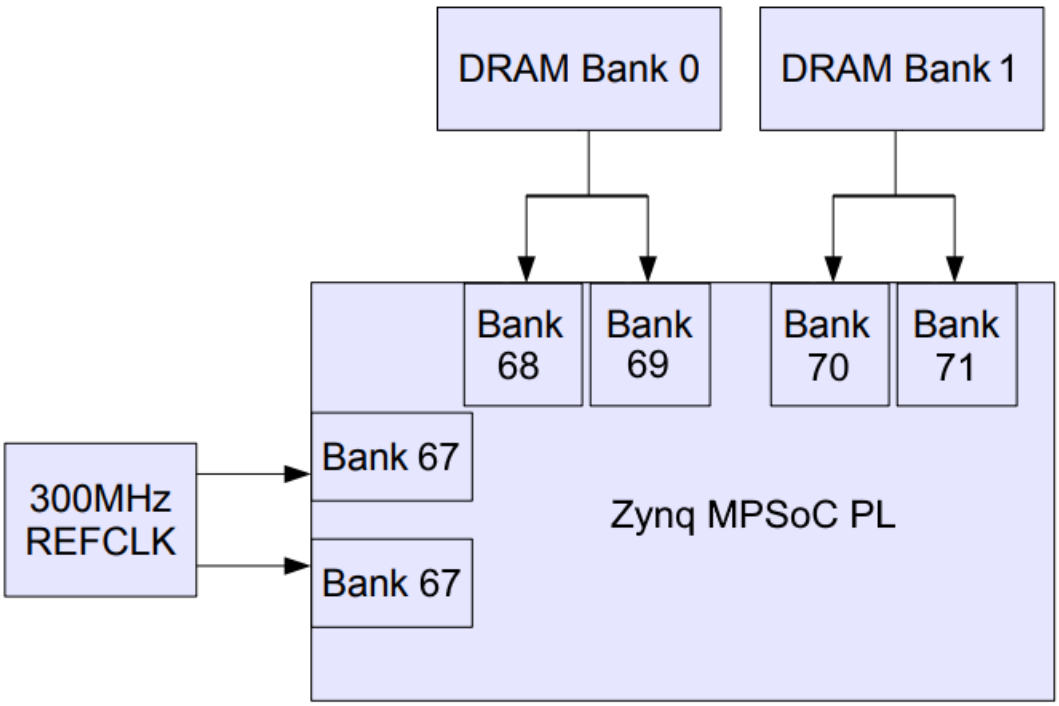


Figure 13 : PL DRAM Banks

3.7.3 MGT Links

There are a total of 18 Multi-Gigabit Transceiver (MGT) links are connected to the FPGA, and 4 links to the PS:

For MGT Clocking see Board Clock Diagram:

The connections of these links are shown in MGT Links:

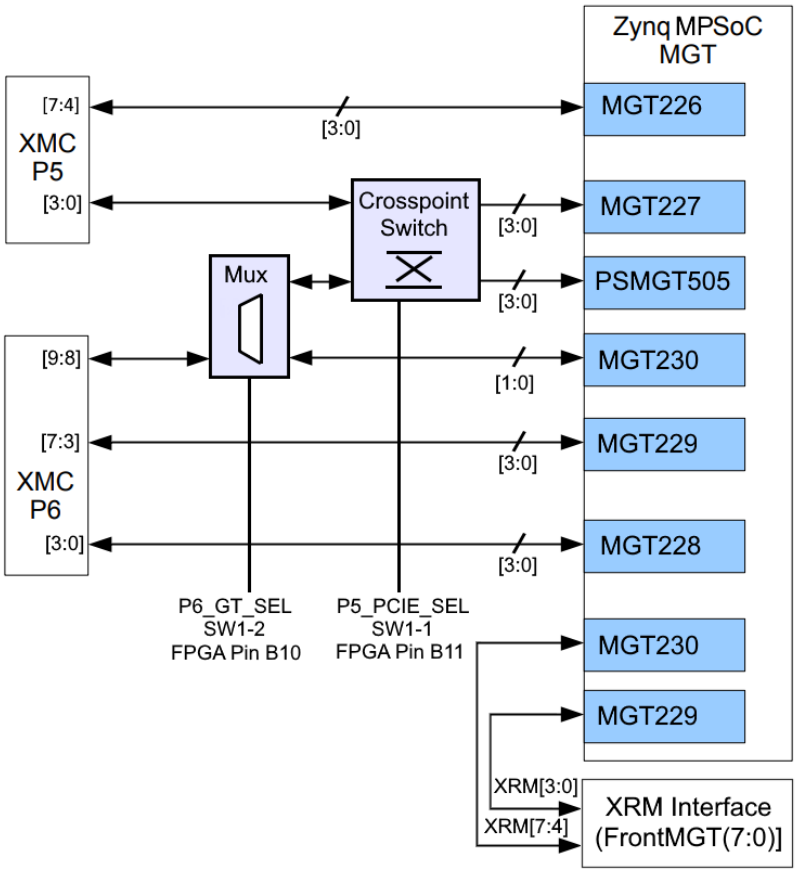


Figure 14 : MGT Links

The transceiver routing is controlled by a crosspoint switch, which selects whether the PS or PL provides the main PCIe[3:0] interface on P5, and a multiplexer, selects between the PS or PL for P6 lanes [1:0]

SW1-1 Controls the P5 crosspoint switch, SW1-2 controls the P6 multiplexer

SW1-2	SW1-1	P6[9:8] Connection	P5[3:0] connection
OFF	OFF	PL MGT230[1:0]	PL MGT227[3:0]
OFF	ON	PL MGT230[1:0]	PS MGT505[3:0]
ON	OFF	PS MGT505[3:2]	PL MGT227[3:0]
ON	ON	PL MGT227[3:2]	PS MGT505[3:0]

Table 14 : MGT Switch Selections

3.7.4 PL GPIO

There are 38 single ended GPIO pins from the FPGA to the P6 connector, which are compatible with 3.3V signalling such as TTL and CMOS. These GPIO pins are passed through a Texas Instruments TXS0108E level translator, capable of open-drain and push-pull level translation. The level translator is auto direction sensing. The level translator has a propagation delay of 5.7ns max and a channel-to-channel skew (within a package) of 1ns. It is suitable for rates up to ~50Mb/s.

There are 6 differential (12 single ended) GPIO pins from the FPGA to the P4 connector. These pins connect to a 1.8V FPGA IO bank, so care must be taken to ensure that they are not over driven. There is an analogue bus switch to protect the FPGA, which is enabled with SW1-6, FPGA pin A11 or using the AVR system monitor.

The P6 GPIO pin mapping is shown in Pn6 GPIO Pin Map, and P4 GPIO is shown in PMC Connector P4.

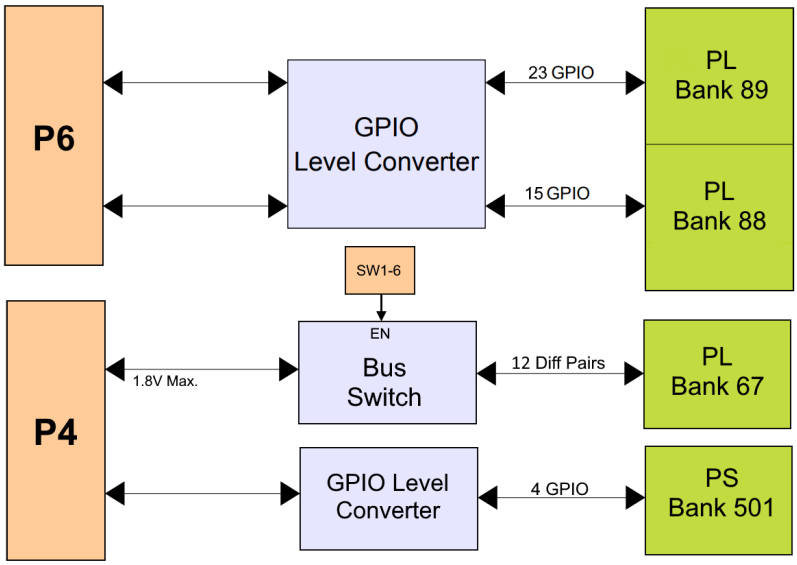


Figure 15 : GPIO Block Diagram

3.8 Configuration

3.8.1 Power-Up Sequence

At power-up, the PS will load the first-stage bootloader from the memory interface selected by the Boot Mode select switches.

The first stage bootloader is responsible for configuring the FPGA and PS attached interfaces.

> **Note:**
> If an over-temperature alert is detected from the System Monitor, the FPGA **will be cleared** by pulsing its PROG signal. See Automatic Temperature Monitoring.

3.9 System Monitoring

The ADM-XRC-9Z1 has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares the information with the PS.

See section Serial COM Portsfor more details about the physical interface.

The following voltage rails and temperatures are monitored:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12.0V	Board Input Supply
5.0V	Internally generated 5V supply
3.3V	Board Input Supply
3.3V	Internally generated 3.3V supply
1.8V	Internally generated 1.8V supply
0.85V	FPGA Core Supply (VccINT)
1.2V	DDR4 SDRAM, memory I/O
0.6V	DRAM VTT Supply
2.5V	Internally generated 2.5V supply
XRM_VIO	Variable XRM IO supply
1.8V	PS VCC aux supply
1.8V	PL MGT Termination supply
0.85V	PS MGT AVCC supply
Temp0	Microcontroller on-die temperature
Temp1	Board temperature sensor on-die temperature
Temp2	FPGA on-die temperature

Table 15 : Voltage and Temperature Monitors

3.9.1 Automatic Temperature Monitoring

The onboard system monitor microcontroller contains pre-programmed temperature limits. The temperature limits are shown in Table Temperature Limits:

	Target FPGA		Bridge FPGA		Board	
	Min	Max	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+85 degC	0 degC	+85 degC
Extended	0 degC	+100 degC	0 degC	+100 degC	0 degC	+100 degC
Industrial	-40 degC	+100 degC	-40 degC	+100 degC	-40 degC	+100 degC

Table 16 : Temperature Limits

Important:

If either FPGA temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by the Green LED (Target Configured or DONE) switching off and the two status LEDs showing a temperature fault indication. This condition is cleared with a power cycle.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang" as a result of communication errors.

An overtemperature shutdown will not occur until the system monitor reads 5 degC above the maximum limit for multiple samples in a row (i.e. +105 degC for Industrial boards). This is to compensate for potential errors in the temperature readings. There is no protection mechanism in place for minimum temperatures or the "Board" temperature sensor limits.

3.9.2 Microcontroller Status LEDs

LEDs D12 (Red) and D11 (Green) indicate the microcontroller status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 17 : Status LED Definitions

3.9.3 System Monitor Interfaces

There are two ways to communicate with the System Monitor to retrieve board status information on the ADM-XRC-9Z1. One is through the Micro USB connector (shown in USB Interfaces), the other is using one of the PS UART interfaces (shown in Serial COM Ports). These communication interfaces are intended to be used with Alpha-Data utility called avr2util. Avr2util is provided with the 9Z1 PetaLinux BSP, and can be run from the ADM-XRC-9Z1 once booted.

To see available options, run:

```
avr2util -?
```

To display sensor values (use -psuart for the PS UART interface, or -usbcom for the MicroUSB interface):

```
avr2util -psuart /dev/ttyPS1,170000 display-sensors
```

To set the user-programmable clock (e.g. PROGCLK at index 1) to 156.25MHz:

```
avr2util -psuart /dev/ttyPS1,170000 setclknv 1 156250000
```

Clock	Index
PCIEREFCLK	0
PROGCLK	1
REFCLK300M	2
FABRIC_CLK	3

Table 18 : avr2util clock indexes

Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

.	A	B	C	D	E	F
1:	PET_P0	PET_N0	3V3	PET_P1	PET_N1	VPWR
2:	GND	GND	-	GND	GND	MRSTI_L
3:	PET_P2	PET_N2	3V3	PET_P3	PET_N3	VPWR
4:	GND	GND	TCK	GND	GND	MRSTO_L
5:	PET_P4	PET_N4	3V3	PET_P5	PET_N5	VPWR
6:	GND	GND	TMS	GND	GND	12V0
7:	PET_P6	PET_N6	3V3	PET_P7	PET_N7	VPWR
8:	GND	GND	TDI	GND	GND	M12V0
9:	-	-	-	-	-	VPWR
10:	GND	GND	TDO	GND	GND	GA0
11:	PER_P0	PER_N0	MBIST_L	PER_P1	PER_N1	VPWR
12:	GND	GND	GA1	GND	GND	MPRESENT_L
13:	PER_P2	PER_N2	3V3_AUX	PER_P3	PER_N3	VPWR
14:	GND	GND	GA2	GND	GND	I2C_SDA
15:	PER_P4	PER_N4	-	PER_P5	PER_N5	VPWR
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	PER_P6	PER_N6	-	PER_P7	PER_N7	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK0_P	REFCLK0_N	-	WAKE_L	ROOT0_L	-

Table 19 : Pn5 Interface

Appendix A.2: Secondary XMC Connector, P6

.	A	B	C	D	E	F
1:	PN6_TX_P0	PN6_TX_N0	GPIO_37	PN6_TX_P1	PN6_TX_N1	GPIO_38
2:	GND	GND	GPIO_35	GND	GND	GPIO_36
3:	PN6_TX_P2	PN6_TX_N2	GPIO_33	PN6_TX_P3	PN6_TX_N3	GPIO_34
4:	GND	GND	GPIO_31	GND	GND	GPIO_32
5:	PN6_TX_P4	PN6_TX_N4	GPIO_29	PN6_TX_P5	PN6_TX_N5	GPIO_30
6:	GND	GND	GPIO_27	GND	GND	GPIO_28
7:	PN6_TX_P6	PN6_TX_N6	GPIO_25	PN6_TX_P7	PN6_TX_N7	GPIO_26
8:	GND	GND	GPIO_23	GND	GND	GPIO_24
9:	PN6_TX_P8	PN6_TX_N8	GPIO_21	PN6_TX_P9	PN6_TX_N9	GPIO_22
10:	GND	GND	GPIO_19	GND	GND	GPIO_20
11:	PN6_RX_P0	PN6_RX_N0	GPIO_17	PN6_RX_P1	PN6_RX_N1	GPIO_18
12:	GND	GND	GPIO_15	GND	GND	GPIO_16
13:	PN6_RX_P2	PN6_RX_N2	GPIO_13	PN6_RX_P3	PN6_RX_N3	GPIO_14
14:	GND	GND	GPIO_11	GND	GND	GPIO_12
15:	PN6_RX_P4	PN6_RX_N4	GPIO_9	PN6_RX_P5	PN6_RX_N5	GPIO_10
16:	GND	GND	GPIO_7	GND	GND	GPIO_8
17:	PN6_RX_P6	PN6_RX_N6	GPIO_5	PN6_RX_P7	PN6_RX_N7	GPIO_6
18:	GND	GND	GPIO_3	GND	GND	GPIO_4
19:	N6_REFCLK_P*	PN6_REFCLK_N*	GPIO_1	PN6_RX_P9	PN6_RX_N9	GPIO_2

Table 20 : Pn6 Interface

Appendix A.2.1: Pn6 GPIO Pin Map

Signal	FPGA Pin	FPGA Bank	IO Standard
GPIO_1	K13	89	LVCMOS33
GPIO_2	H13	89	LVCMOS33
GPIO_3	L13	99	LVCMOS33
GPIO_4	J12	89	LVCMOS33
GPIO_5	L12	89	LVCMOS33
GPIO_6	G13	89	LVCMOS33
GPIO_7	K12	88	LVCMOS33
GPIO_8	H14	89	LVCMOS33
GPIO_9	J10	88	LVCMOS33
GPIO_10	J14	89	LVCMOS33
GPIO_11	G11	88	LVCMOS33
GPIO_12	K14	89	LVCMOS33
GPIO_13	H11	88	LVCMOS33
GPIO_14	J11	88	LVCMOS33
GPIO_15	G10	88	LVCMOS33
GPIO_16	K10	88	LVCMOS33
GPIO_17	F11	88	LVCMOS33
GPIO_18	H12	88	LVCMOS33
GPIO_19	F13	89	LVCMOS33
GPIO_20	F10	88	LVCMOS33
GPIO_21	E13	89	LVCMOS33
GPIO_22	E12	88	LVCMOS33
GPIO_23	D11	88	LVCMOS33
GPIO_24	F12	88	LVCMOS33
GPIO_25	E14	89	LVCMOS33
GPIO_26	E10	88	LVCMOS33
GPIO_27	B13	89	LVCMOS33
GPIO_28	D14	89	LVCMOS33
GPIO_29	A13	89	LVCMOS33
GPIO_30	C13	89	LVCMOS33
GPIO_31	B14	89	LVCMOS33
GPIO_32	C14	89	LVCMOS33
GPIO_33	F15	89	LVCMOS33
GPIO_34	A15	89	LVCMOS33
GPIO_35	E15	89	LVCMOS33

Table 21 : Pn6 GPIO Pin Map (continued on next page)

Signal	FPGA Pin	FPGA Bank	IO Standard
GPIO_36	B15	89	LVCMOS33
GPIO_37	D15	89	LVCMOS33
GPIO_38	G14	89	LVCMOS33

Table 21 : Pn6 GPIO Pin Map

Appendix A.3: PMC Connector P4

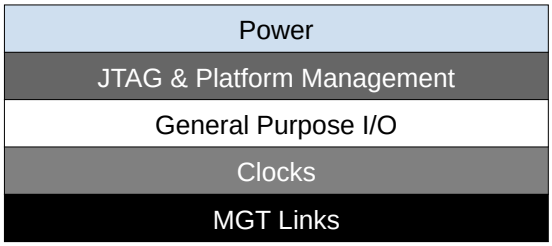
Signal	FPGA Pin	P4 Pin	P4 Pin	FPGA Pin	Signal
ETH0_MDI0_P	-	1	2	-	ETH0_MDI2_P
ETH0_MDI0_N	-	3	4	-	ETH0_MDI2_N
GND	-	5	6	-	GND
ETH0_MDI1_P	-	7	8	-	ETH0_MDI3_P
ETH0_MDI1_N	-	9	10	-	ETH0_MDI3_N
GND	-	11	12	-	GND
ETH1_MDI0_P	-	13	14	-	ETH1_MDI2_P
ETH1_MDI0_N	-	15	16	-	ETH1_MDI2_N
GND	-	17	18	-	GND
ETH1_MDI1_P	-	19	20	-	ETH1_MDI3_P
ETH1_MDI1_N	-	21	22	-	ETH1_MDI3_N
GND	-	23	24	-	GND
USB1_DM		25	26	-	USB2_DM
USB1_DP		27	28	-	USB2_DP
USB1_VBUS		29	30	-	USB2_VBUS
GND	-	31	32	-	GND
P4_GPIO4_P	AL25	33	34	AN22	P4_GPIO2_P
P4_GPIO4_N	AM25	35	36	AP22	P4_GPIO2_N
P4_GPIO1_P	AM26	37	38	-	GND
P4_GPIO1_N	AN26	39	40	M34(MIO30)*	COM1_RXN
COM1_TXN	M35(MIO31)*	41	42	M34(MIO30)*	COM1_RXP
COM1_TXP	M35(MIO31)*	43	44	-	GND
COM2_TXN	AW26	45	46	AW27	COM2_RXN
COM2_TXP	AW26	47	48	AW27	COM2_RXP
GND	-	49	50	-	GND
CANH	K37/L33 (MIO26/27)*	51	52	AL22	P4_GPIO3_P
CANL	K37/L33 (MIO26/27)*	53	54	AL23	P4_GPIO3_N
GND	-	55	56	AM23	P4_GPIO5_P
P4_GPIO6_P	AK24	57	58	AM24	P4_GPIO5_N
P4_GPIO6_N	AK25	59	60	K35(MIO36)	PS_GPIO3
PS_GPIO1	L32(MIO34)	61	62	M33(MIO37)	PS_GPIO4
PS_GPIO2	K34(MIO35)	63	64	-	GND

Table 22 : Pn4 Interface

* These FPGA pins are not connect directly to the FPGA, but instead go through an on-board transceiver/.

Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



Appendix B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	AW21	1	2	AT16	DA_N1
DA_P0	AV21	3	4	AT17	DA_P1
DA_N2	AL17	5	6	AP20	DA_P3
DA_P2	AL18	7	8	AR20	DA_N3
DA_N4	AU21	9	10	AW16	DA_N5
DA_P4	AT21	11	12	AV16	DA_P5
DA_N6	AM18	13	14	AU20	DA_N7
DA_P6	AM19	15	16	AT20	DA_P7
DA_P8	AN21	17	18	AV17	DA_P9
DA_N8	AP21	19	20	AW17	DA_N9
DA_N10	AT18	21	22	AR19	DA_N11
DA_P10	AR18	23	24	AP19	DA_P11
DA_N12	AM21	25	26	AW20	DA_P13
DA_P12	AL21	27	28	AW19	DA_N13
DA_N14	AV19	29	30	AU18	DA_P15
DA_P14	AU19	31	32	AV18	DA_N15
DB_N0	AJ19	33	34	AP16	DB_N1
DB_P0	AH19	35	36	AN16	DB_P1
SA_0	AM20	37	38	AP17	DA_CC_P16
3V3	-	39	40	AN17	DA_CC_N16
3V3	-	41	42	-	FORCE2V5_L
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
PRESENCE_L	-	55	56	-	TDI
TCK	-	57	58	-	TRST
TMS	-	59	60	-	TDO

Table 23 : XRM Connector CN1, Field 1

Appendix B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	AG19	61	62	AH21	DB_N3
DB_P2	AG20	63	64	AG21	DB_P3
DB_N4	AU13	65	66	AN12	DB_N5
DB_P4	AU14	67	68	AN13	DB_P5
DB_N6	AJ20	69	70	AW12	DB_N7
DB_P6	AJ21	71	72	AV12	DB_P7
DB_N8	AM14	73	74	AW15	DB_P9
DB_P8	AL15	75	76	AW14	DB_N9
DB_P10	AK19	77	78	AW10	DB_N11
DB_N10	AK18	79	80	AW11	DB_P11
DB_N12	AN14	81	82	AV14	DB_P13
DB_P12	AM15	83	84	AV13	DB_N13
DB_N14	AL20	85	86	AV11	DB_N15
DB_P14	AK20	87	88	AU11	DB_P15
DB_CC_P16	AP15	89	90	AT15	SB_1
DB_CC_N16	AR15	91	92	AL12	SC_0
SA_1	AR17	93	94	AH17	SC_1
SB_0	AH18	95	96	AW5	SD_0
DC_CC_P16	AP14	97	98	AT11	DC_N1
DC_CC_N16	AR14	99	100	AT12	DC_P1
DC_N0	AL10	101	102	AU6	DD_CC_P16
DC_P0	AK10	103	104	AV6	DD_CC_N16
SD_1	AR8	105	106	AM11	SD_3
SD_2	AP6	107	108	AV7	GCLK_M2C_N
MGTCLK_M2C_P	AH10	109	110	AV8	GCLK_M2C_P
MGTCLK_M2C_N	AH9	111	112	-	SDA
XRM_LVDS_C-LK_N	AN19	113	114	-	SCL
XRM_LVDS_C-LK_P	AN18	115	116	-	ALERT_N
MGT_C2M_P7	AE8	117	118	AE4	MGT_M2C_P7
MGT_C2M_N7	AE7	119	120	AE3	MGT_M2C_N7

Table 24 : XRM Connector CN1, Field 2

Appendix B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	AP12	121	122	AH14	DC_P3
DC_N2	AR12	123	124	AJ14	DC_N3
DC_N4	AT13	125	126	AJ17	DC_P5
DC_P4	AR13	127	128	AK17	DC_N5
DC_P6	AK14	129	130	AJ12	DC_P7
DC_N6	AK13	131	132	AK12	DC_N7
DC_N8	AM10	133	134	AJ16	DC_N9
DC_P8	AL11	135	136	AH16	DC_P9
DC_P10	AT10	137	138	AP10	DC_N11
DC_N10	AU10	139	140	AP11	DC_P11
DC_P12	AR10	141	142	AK15	DC_N13
DC_N12	AR9	143	144	AJ15	DC_P13
DC_N14	AP8	145	146	AU9	DD_P1
DC_P14	AP9	147	148	AU8	DD_N1
DD_P0	AT8	149	150	AM13	DC_N15
DD_N0	AT7	151	152	AL13	DC_P15
DD_P2	AP7	153	154	AW6	DD_N3
DD_N2	AR7	155	156	AW7	DD_P3
DD_N4	AT5	157	158	AP4	DD_N5
DD_P4	AT6	159	160	AP5	DD_P5
DD_P6	AR3	161	162	AU4	DD_N7
DD_N6	AT3	163	164	AU5	DD_P7
DD_N8	AW4	165	166	AT2	DD_N9
DD_P8	AV4	167	168	AR2	DD_P9
DD_N10	AU1	169	170	AV3	DD_N11
DD_P10	AT1	171	172	AU3	DD_P11
DD_N12	AW2	173	174	AP1	DD_N13
DD_P12	AV2	175	176	AP2	DD_P13
DD_N14	AW9	177	178	AR4	DD_N15
DD_P14	AV9	179	180	AR5	DD_P15

Table 25 : XRM Connector CN1, Field 3

Appendix B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
MGT_C2M_P0	AM6	1	2	AM2	MGT_M2C_P0
MGT_C2M_N0	AM5	3	4	AM1	MGT_M2C_N0
MGT_C2M_P1	AL8	5	6	AL4	MGT_M2C_P1
MGT_C2M_N1	AL7	7	8	AL3	MGT_M2C_N1
MGT_C2M_P4	AH6	9	10	AH2	MGT_M2C_P4
MGT_C2M_N4	AH5	11	12	AH1	MGT_M2C_N4
MGT_C2M_P5	AG8	13	14	AG4	MGT_M2C_P5
MGT_C2M_N5	AG7	15	16	AG3	MGT_M2C_N5
MGT_C2M_P2	AK6	17	18	AK2	MGT_M2C_P2
MGT_C2M_N2	AK5	19	20	AK1	MGT_M2C_N2
MGT_C2M_P3	AJ8	21	22	AJ4	MGT_M2C_P3
MGT_C2M_N3	AJ7	23	24	AJ3	MGT_M2C_N3
MGT_C2M_P6	AF6	25	26	AF2	MGT_M2C_P6
MGT_C2M_N6	AF5	27	28	AF1	MGT_M2C_N6

Table 26 : XRM Connector CN2

Revision History

Date	Revision	Nature of Change	Section
11 Jan 2022	0.1	Initial Draft	N/A
04 Jul 2022	1.0	First release, fixing some minor errors	N/A
16 Feb 2023	1.1	Update "P5/P6 GT Sel" link to point to correct table	N/A
10 May 2023	1.2	Clarified UART connections between PS and PL, Added Ethernet LED defintions, Updated PS reset switch definition.	N/A
08 Jun 2023	1.3	Removed dead link to heatsink environmental specifications	N/A
21 Jun 2023	1.4	Corrected FPGA pin number for MRSTI and corrected PS MIO pin number for PS GPIO	Section 3.3.4, Section 3.6.10
30 Aug 2023	1.5	Clarified 3V3_AUX power sequence requirement is only when boot mode pins are overridden	Section 3.1.1
03 Oct 2023	1.6	Added heatsink performance vs airflow graph	Section 2.1.3
05 Oct 2023	1.7	Added MRSTO circuit diagram and description of SW1-5	Section 3.3.5
19 Jan 2024	1.8	Added link to serial interface section from the system monitoring section, updated heatsink performance vs airflow with new heatsink revision.	Section 3.9, Section 2.1.3

Address: Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 10822 West Toller Drive, Suite 250 Littleton, CO 80127
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com